IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicant	:	Stephen R. Van Doren, et al.
Serial No.	:	10/760,640
Filing Date	:	January 20, 2004
For	:	CACHE COHERENCY PROTOCOL WITH ORDERING POINTS
Group Art Unit	:	2188
Confirmation No.	:	9874
Examiner	:	Mardochee Chery
Attorney Docket No.	:	200313588-1

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REPLY BRIEF

Sir:

This Reply Brief is in response to the Examiner's Answer dated August 13, 2010. This Reply Brief addresses the Examiner's Answer concerning the appealed claims 1-9, 11-13 and 15-24.

I. **Preliminary Comments**

On pages 16-18 of the Examiner's Answer dated August 22, 2008 (hereinafter, "Examiner's Answer"), the Examiner's Answer cites an extensive amount of law with virtually no analysis or application of the cited law in relation to the present application or the claims. As an example, on pages 16-17, the Examiner's Answer recites claim 1, then recites case law which holds that an intended use of an apparatus claim does not distinguish the claim over a prior art apparatus (See Examiner' Answer, Page 17, citing *In re Otto*, *In re Sinex* and *In re Schriber*). However, the Examiner's Answer fails to explain how such law supports the Examiner's interpretation of claim 1. Instead, the Examiner's Answer simply recites the law, and then abruptly changes topics (See Examiner's Answer, Page 18). From the Examiner's Answer Appellant's representative cannot discern which features of the claims the Examiner's Answer is contending constitutes a mere "intended use."

Nothing in the case law cited in the Examiner's Answer on pages 16-18 would even indicate that claims 1-9, 11-13 and 15-24 are directed to an intended use. For instance, in *in re Otto*, the intended use was recited in the preamble of the claim under consideration. *In re Otto*, 312 F.2d 937, 136 U.S.P.Q. 458-459 (C.C.P.A. 1963). A similar situation also occurred in *In re Sinex* and *In re Schriber*, as in both cases, the preamble of the claim recited an intended use. *In re Sinex*, 309 F.2d 488, 135 U.S.P.Q. 302 (C.C.P.A. 1062) and *In re Schriber* 128 F.3d 1473, 44 U.S.P.Q.2d 1429, 1431 (Fed. Cir. 1997). In the present case, claims 1-9, 11-13 and 15-24 do not recite an intended use in a preamble. Instead, the preamble of claims 1-9 and 15-18 recite a system, the preamble of claims 11-13 recite a multi-processor network, the preamble of claims 19-23 recite a method and claim 24 recites a coherency protocol.

Moreover, on page 16 of the Examiner's Answer, it appears that the entire basis for holding that the claims recite an intended use is related to the recitation of the term "capable of" in claim 1. However, the term "capable of" is not a recitation of an intended use or optional, but instead recites an explicit property that results from the cache state; namely, that the cache state, which is a property of a first node, confers a particular capacity or ability onto the first node (as opposed to the system disclosed in Glasco which does not have such capacity or ability). Similar claim

language existed and was not objected to in the recently decided CAFC opinion of *Golden Hour Data Systems, Inc. v. emsCharts, Inc.*, ___ F.3d___ (Fed. Cir. 2010).

Significantly, independent claims 15, 19 and 24 do not include the term "capable of," such that the intended use rationale being espoused against these claims is not applicable. That is, claims 15, 19 and 24 recite different systems and methods and therefore must be considered separately from claim 1. Additionally, claim 15 is a means-plus-function claim, which under 35 U.S.C. §112, sixth paragraph, is directed to the corresponding structure, material, or acts described in the specification and equivalents thereof. In section L on page 8 of the Appeal Brief, examples of the structure (e.g., not intended use) disclosed in the Specification corresponding to the elements recited in claim 15 is noted. Further, claim 19 is directed to a method that recites specific acts, and not a mere intended use. Claim 24 is directed to a system and also does not include the "capable of" language emphasized in the Examiner's Answer. Therefore, there is no basis to dismiss claims 15, 19 and 24 as being directed to an "intended use" as contended by the Examiner's Answer regarding claim 1. The arguments in Appellant's Appeal Brief at pages 11-15 demonstrate further differences between independent claims 15, 19 and 24 and U.S. Patent Pub. No. 2005/0251626 to Glasco.

II. Appealed Claim 1

On pages 12-15 of the Appeal Brief, Appellant's representative set forth reasons that U.S. Patent Pub. No. 2005/0251626 to Glasco (hereinafter, "Glasco") fails to disclose the first node recited in claim 1. The Examiner's Answer argues that Pars. [0033] and [0042] of the Specification of the present application are similar to Pars. [0087], [0091], [0016] and [0120]-[0123] of Glasco (See pages 9-10 of the Examiner's Answer). In particular, the Examiner's Answer appears to argue that in Glasco, a cache line having a modified (M), owned (O) or dirty (D) state indicates that the cache line defines an ordering point (See Examiner's Answer, Page 10). Appellant's representative respectfully disagrees. The Specification states that the state of cached data defines a node as a cache ordering point for the data (See Spec., Par. [0042], citied by the Examiner's Answer). This statement in the Specification is describing a specific embodiment of a system within the scope of the present application and not what is known in the prior art. Appellant's representative

respectfully submits that a cache line having a 'M', 'O' or 'D' state in the context of Glasco in no way indicates (by itself) that the cache line is an ordering point for data.

Furthermore, as noted by the Examiner's Answer, on page 15, although claims are interpreted in light of the specification, limitations from the specification are not read into the claims. *In re Van Geuns*, 988 F.2d 1181, 1184, 26 U.S.Q.2d 1057 (Fed. Cir. 1993). Thus, arguments made in the Examiner's Answer regarding the Specification are not relevant, as the Examiner's Answer is seeking to read limitations into the claims from the Specification, which are not recited in claim 1.

Additionally, the Examiner's Answer appears to contend that in Glasco, a cache line having a modified (M), owned (O) or dirty (D) state reads on the first node recited in claim 1 (See Examiner's Answer, Page 10). To support this contention, the Examiner's Answer cites Par. [0065] of Glasco, which states that a cache controller 509 accepts probes from a local memory and forwards the probe to non-local nodes 511 (See Examiner's Answer, Page 11). In claim 1, the recited first node has a cache including data having an associated first cache state, the first cache state being capable of identifying the first node as being an ordering point for serializing requests from other nodes for the data. That is, in claim 1, the recited cache includes data having the associated first cache state. In the cited section of Glasco, the cache coherence controller 509 does not include data having an associated first cache state, in contrast to the first node recited in claim 1. Instead, the cache coherence controller 509 forwards probes from a local memory controller 503-1 to non-local nodes 511. Obviously, in Glasco there would be no reason for the cache coherence controller 509 to forward the probe if the cache coherence controller included data requested by the probe. Thus, Appellant's representative maintains that no structure or process disclosed in Glasco reads on the first node recited in claim 1.

Additionally, the Appeal Brief demonstrated that in claim 1 it is data in an associated cache of the first node that identifies the first node as the ordering point such that it can serialize requests from other nodes, whereas in Glasco, it is the entries in a coherence directory of a memory controller for multiple processors that indicate the state of the line (See Appeal Brief, Page 15). In response, the Examiner's Answer stated the following:

> [a]s evident from the claim language itself "...the first cache state {is what is} being capable of identifying the first node as being an ordering point for serializing requests from other nodes for the data." Thus, there is "an associated cache which includes data" and there is (a) "cache state associated with that data." In claim 1, it is "the state of the cache" that identifies the node as the ordering point "not the data in the associated cache" as assumed by appellant. Examiner's Answer, Page 12.

Appellant's representative respectfully submits that the response proffered in the Examiner's Answer illustrates that claim 1 has been misconstrued. The cache state (which the Examiner's Answer admits identifies a node as an ordering point) inherently has data that defines the cache state. Moreover, since the cache state is associated with data included in the associated cache, Appellant's representative maintains that, in claim 1, data having the cache state in the associated cache of the first node identifies the first node as the ordering point. No such node in Glasco has data in a particular cache state such that the node is identified as an ordering point consistent with claim 1.

Moreover, to anticipate a claim, a reference must disclose every element of the challenged claim and enable one skilled in the art to make the anticipating subject matter. *PPG Indus. v. Guardian Indus. Corp.*, 75 F.3d 1558, 1566, 37 USPQ2d 1618, 1624 (Fed. Cir. 1996) citing *Chester v. Miller*, 906 F.2d 1574, 1576, 15 U.S.P.Q.2d (BNA) 1333, 1336 (Fed. Cir. 1990). Appellant's representative respectfully submits that, as explained above in the Appeal Brief, Glasco does not disclose every element and enable one of ordinary skill in the art to make the system recited in claim 1, and thus, Glasco cannot anticipate claim 1. Accordingly, claim 1 is patentable and reversal of the rejection of claim 1 is respectfully requested.

III. Appealed Claim 2

On pages 16-17 of the Appeal Brief, Appellant's representative set forth reasons that Glasco does not disclose that a first cache state enables a first node to provide a data response to a request for the data from a second node without updating a system memory, as recited in claim 2. In response, the Examiner's Answer stated the following:

> Glasco teaches "in a cluster system, requests are generated to specific processors to invalidate cache entries and to write cache entries back to memory; if the directory indicates that the line is in the dirty state in any of the remote caches, the modified memory line to memory **must be written to back to memory** before the line is invalidated in each of the remote caches; paragraphs [0016, 0018, 0120]." Examiner's Answer, Page 13 (emphasis added).

Appellant's representative respectfully submits that the above statement supports the patentability of claim 2. The cited sections of Glasco merely disclose situations where a write-back to memory is performed. Conversely, claim 2 recites that the first cache state enables the first node to provide the data response to a request for the data from the second node without updating a system memory (e.g., no write-back is performed), as recited in claim 2. Thus, Appellant's representative maintains that Glasco does not anticipate claim 2 since Glasco does not disclose the subject matter recited in claim 2. Therefore, for the reasons stated above, as well as the reasons given in the Appeal Brief, Appellant's representative respectfully requests reversal of the rejection of claim 2.

IV. Appealed Claim 3

On pages 17-18 of the Appeal Brief, Appellant's representative set forth reasons that the Final Action issued on April 29, 2010 did not identify any structure or function in Glasco that enables a first node to provide an ownership data response to a request for data from a second node, the ownership data response transferring an ordering point from the first node to the second node, the ownership data response comprising a copy of the data requested from the second node, as recited claim 3. In response, the Examiner's Answer stated the following:

> Glasco teaches "in a clustering system, requests are generated to specific processors to invalidate cache entries and to write cache entries back to memory; if the directory indicates that the line is in the dirty state in any of the remote caches, the modified memory line to memory must be written back to memory before the line is invalidated in each of the remote caches; paragraphs [0016, 0018, 0120]. Examiner's Answer, Page 13.

The cited sections of Glasco merely disclose situations where a write-back to memory is performed. Conversely, claim 3 recites that the ordering point is transferred from the first node to the second node as an ownership data response that includes a copy of the data requested from the second node. Significantly, the cited sections of Glasco are completely silent on the status of an ordering point. Thus, Appellant's representative maintains that Glasco does not anticipate claim 3 since Glasco does not disclose the subject matter recited in claim 3. For the reasons stated above, as well as the reasons given in the Appeal Brief, Appellant's representative respectfully requests reversal of the rejection of claim 3.

V. Appealed Claim 5

On pages 18-19 of the Appeal Brief, Appellant's representative set forth reasons that the Final Action failed to identify structure that enable communication between processors, in contrast to the system interconnect recited in claim 5. The Examiner's Answer fails to address the arguments made by Appellant's representative regarding the patentability of claim 5. Thus, Appellant's representative respectfully submits that for the reasons given in the Appeal Brief, Glasco does not anticipate claim 5. Therefore, Appellant's representative maintains that claim 5 is patentable, and reversal of the rejection of claim 5 is respectfully requested.

VI. Appealed Claim 7

On pages 20-22 of the Appeal Brief, Appellant's representative set forth reasons that Glasco taken in view of U.S. Patent No. 6,138,218 to Arimilli et al. ("Arimilli") fails to teach or suggest that a system implements a hybrid cache coherency protocol, as recited in claim 7. In response, the Examiner's Answer stated the following:

> Arimilli discloses "snoop operations which are retired and making forward progress on retired snoop operations; col. 1, lines 13-14; coherency of the storage hierarchy is maintained through the use of a selected memory coherency protocol such as the MESI protocol; the coherency state is indicated by bits in the cache directory; col. 1, lines 33-41; and in FIG. 2A-2C, a mechanism for making forward progress on a retried snoop; a first device initiates a read or writm operation, upon detection of the read or rwitm operation I2 cache

> asserts an intervention response, however, the intervention response is impeded by a second device, asserting a retry; I2 cache 114 initiates an action altering the coherency state associated with a requested cache item or initiates a push operation to write (modified) the requested cache item; the push operation may be snooped off the system bus by other devices; col. 5, lines 19-54. Examiner's Answer Pages 14-15.

Appellant's representative respectfully submits that the above response fails to identify any protocol that corresponds to the Hybrid protocol recited in claim 7. The hybrid protocol recited in claim 7 is configured such that first and second processors employs a source broadcast-based protocol to issue a request for data and employs an associated forward progress protocol to reissue a request for the data if the request fails in the source broadcast protocol. Instead, the Examiner's Answer merely cites sections of Arimilli that disclose procedures for making forward progress toward a final state. Making forward progress does not inherently require, teach or suggest the employment of a forward progress protocol, as recited in claim 7. Therefore, for the reasons stated above, as well as those discussed in the Appeal Brief, claim 7 is patentable over Glasco taken in view of Arimilli, since Glasco taken in view of Arimilli fails to teach or suggest any structure or process that corresponds to the hybrid protocol recited in claim 7, and no other evidence has been provided in the Examiner's Answer sufficient to support the obviousness position. Thus, reversal of the rejection of claim 7 is respectfully requested.

VII. Appealed Claim 8

On page 22 of the Appeal Brief, Appellant's representative set forth reasons that Glasco taken in view of Arimilli fails to teach or suggest that a forward progress protocol comprises a null-directory, as recited in claim 8. In response, the Examiner's Answer cites the same sections of Arimilli that were used in the Examiner's Answer regarding claim 7 (See Examiner's Answer, Page 16). However, for reasons discussed above with respect to claim 7, the cited sections of Arimilli fail to teach or suggest either the forward progress protocol, or the null directory protocol recited in claim 8. Accordingly, Appellant's representative maintains that Glasco taken in view of Arimilli fails to teach or suggest the system of claim 8, since Glasco taken in view of Arimilli fails to teach or suggest that a forward progress protocol comprises a null directory protocol, as recited in claim 8. Therefore, for the reasons

stated above, as well as those discussed in the Appeal Brief, reversal of the rejection of claim 8 is respectfully requested.

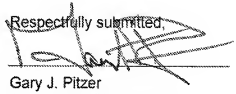
VIII. CONCLUSION

In view of the foregoing remarks, Appellant's representative respectfully requests that the rejection of the appealed claims be reversed and that a Notice of Allowance be issued.

No additional fees should be due for this Reply Brief. In the event any fees are due in connection with the filing of this document, the Commissioner is authorized to charge those fees to Deposit Account No. 08-2025.

I hereby certify that this correspondence is being transmitted to the U.S. Patent and Trademark Office via electronic filing on September 24, 2010.

Respectfully submitted,



Gary J. Pitzer
Registration No. 39,334
Attorney for Appellants

CUSTOMER NO.: 022879

Hewlett-Packard Company
Legal Department MS 79
3404 E. Harmony Road
Ft. Collins, CO 80528